

SC #1089 JCT16 U.S. PTO
10/016232
12/06/01

PATENT NUMBER and
ISSUE DATE

U.S. UTILITY Patent Application

APPL NUM 10016232	FILING DATE 12/06/2001	CLASS 716	SUBCLASS 2	GAU 2825	EXAMINER J. ...
**APPLICANTS: Donelly Ross; Naylor William; Fu Michael;					
**CONTINUING DATA VERIFIED: none any of					
**FOREIGN APPLICATIONS VERIFIED: none any of					
PG-PUB DO NOT PUBLISH <input checked="" type="checkbox"/>			RESCIND <input type="checkbox"/>		
Foreign priority claimed <input type="checkbox"/> yes <input checked="" type="checkbox"/> no			ATTORNEY DOCKET NO		
35 USC 119 conditions met <input type="checkbox"/> yes <input checked="" type="checkbox"/> no			SNSY-A2001-007		
Verified and Acknowledged Examiners's initials 7-11					
TITLE : Multiple pass optimization for automatic electronic circuit placement					
U.S. DEPT. OF COM. / PAT. & TM. PTO-436 (Rev. 12-94)					

NOTICE OF ALLOWANCE MAILED		Assistant Examiner	CLAIMS ALLOWED	
			Total Claims	Print Claim for
ISSUE FEE		Primary Examiner	DRAWING	
Amount Due	Date Paid		Electronic Drwg.	Figs. Drwg.
<input type="checkbox"/> TERMINAL DISCLAIMER		PREPARED FOR ISSUE	Application Examiner	
WARNING: The information disclosed herein may be restricted. Unauthorized disclosure may be prohibited by the United States Code Title 35, Sections 122, 181 and 368, Possession outside the U.S. Patent & Trademark Office is restricted to authorized employees and contractors only.				

FILED WITH:

☐ DISK (CRF)

☐ CD-ROM
(Attached in pocket on right inside flap)

BEST AVAILABLE